AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Currently Amended) A tiedown structure, comprising:

a semiconductor substrate having a chip formed thereon, the chip comprising an electrical device;

a kerf region proximate the chip; and

a conductive connector forming an electrical connection between the chip and the kerf region; wherein the device is grounded by the conductive connector to prevent charge overloading of the device during a processing step.

2. (Original) The tiedown structure of claim 1, further comprising:

an edge seal along an outer perimeter of the chip,

wherein the conductive connector crosses the edge seal.

3. (Original) The tiedown structure of claim 2, wherein the conductive connector is not in electrical communication with the edge seal.

4. (Currently Amended) The tiedown structure of claim 1, wherein the conductive connector is a metal line and the device is a transistor.

5. (Currently Amended) The tiedown structure of claim 1, wherein the processing step includes plasma etching ~~the chip comprises a device and the conductive connector is in electrical communication with the device and the kerf region~~.

6. (Original) The tiedown structure of claim 5, wherein the conductive connector is in electrical communication with ground potential in the kerf region.

7. (Currently Amended) A tiedown structure comprising:

a semiconductor substrate having a chip formed thereon, the chip comprising an electrical device;

an edge seal along an outer perimeter of the chip; and

a conductive connector forming an electrical connection between the edge seal and the device to ground the device and to prevent charge overloading of the device during a processing step ~~a portion of the chip~~.

8. (Currently Amended) The tiedown structure claim 5, wherein the conductive connector is a metal line and the device is a transistor ~~the chip comprises a device and the conductive connector is in electrical communication with the device and the edge seal~~.

9. (Currently Amended) The tiedown structure of claim 7, wherein the conductive connector is a metal line and the device is a transistor.

10. (Currently Amended) A method for forming a ~~tiedown~~ semiconductor structure, comprising:

forming a device on a chip;

defining a kerf proximate the chip; ~~and~~

forming an electrically conductive connector, the conductive connector connecting the device and the kerf for grounding the device during a subsequent processing step;

completing fabrication of the chip including performing the processing step; and

removing an end of the conductive connector from the kerf thereby preventing short circuits to ground of the device during device operation.

11. (Original) The method of claim 10, wherein forming a conductive connector comprises forming a metal line.

12. (Original) The method of claim 10, wherein the conductive connector connecting the device and the kerf connects the device to ground potential in the kerf.

13. (Currently Amended) The method of claim 10, ~~further comprising:~~ wherein the processing step includes plasma etching.

~~removing an end of the conductive connector from the kerf~~.

14. (Currently Amended) The method of claim 10 ~~13~~, wherein removing an end of the conductive connector comprises sawing through the kerf.

15. (Currently Amended) The method of claim 10 ~~13~~, wherein removing an end of the conductive connector comprises etching.

16. (Currently Amended) The method of claim 10 ~~13~~, wherein removing an end of the conductive connector comprises focused ion beam milling.

17. (Currently Amended) A method for forming a ~~tiedown~~ semiconductor structure, comprising:

forming a chip on a semiconductor substrate, the chip including a device;

forming an edge seal along an outer perimeter of the chip; ~~and~~

forming an electrically conductive connector, the conductive connector connecting the edge seal and the device for grounding the device during a processing step;

completing fabrication of the chip including performing the processing step; and

removing a portion of the conductive connector thereby preventing short circuits to ground during device operation.

18. (Original) The method of claim 17, wherein forming a conductive connector comprises forming a metal line.

19. (Original) The method of claim 17, wherein the conductive connector connecting the edge seal and the device connects the device to ground potential in the edge seal.

20. (Currently Amended) The method of claim 17, ~~further comprising:~~ wherein the processing step includes plasma etching ~~removing a portion of the conductive connector~~.

21. (Original) The method of claim 20, wherein removing the portion of the conductive connector comprises removing a portion of the conductive connector between the edge seal and the device.

22. (Original) The method of claim 21, wherein removing the portion of the conductive connector comprises etching.

23. (Original) The method of claim 21, wherein removing the portion of the conductive connector comprises focused ion beam milling.